IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Cheng-Lien Chiang		
Assignee:	Bridge Semiconductor Corporation		
Title:	OPTOELECTRONIC SEMICONDUCTOR PACKAGE DEVICE		
Serial No.:	10/082,500	Filed:	February 25, 2002
Examiner:	Chu, C.	Group Art Unit:	2815
Atty. Docket No.:	BDG005-3		

COMMISSIONER FOR PATENTS
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APPEAL BRIEF
(37 C.F.R. § 1.192)

Dear Sir:

This Appeal Brief is in furtherance of the Notice of Appeal filed concurrently herewith.

Applicant is a small entity. Please charge the $160 fee under 37 C.F.R. § 1.17(c) to Deposit Account No. 502178/BDG005-3 and charge any underpayment or credit any overpayment to this Account.

This paper is submitted in triplicate.

The index of subject matter is as follows:

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Bridge Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

Claims in the application are: 1-150

B. Status of All Claims

1. Claims canceled: NONE
2. Claims withdrawn: NONE
3. Claims pending: 1-150
4. Claims allowed: NONE
5. Claims rejected: 1-150

C. Claims on Appeal

Claims on appeal are: 1-150

IV. STATUS OF AMENDMENTS

No amendment has been filed after the outstanding Office Action dated July 31, 2003.

V. SUMMARY OF INVENTION

The present invention is generally directed to an optoelectronic semiconductor package device (Specification, page 4, lines 2-3).

In accordance with one aspect of the invention, an optoelectronic semiconductor package device includes a semiconductor chip, an insulative housing and a conductive trace, wherein the chip includes an upper surface and a lower surface, the upper surface includes a light sensitive cell and a conductive pad, the insulative housing includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, and the conductive trace extends outside the insulative housing and is electrically connected to the pad inside the insulative housing (Specification, page 4, lines 4-11).

An embodiment of the present invention discloses an optoelectronic semiconductor package device and its method of manufacture. The method includes providing semiconductor chip 110 that includes upper surface 112 and lower surface 114, where upper surface 112 includes light sensitive cell 115 and conductive pads 116 (Specification, page 8, lines 5-11 and Figs. 1A and 1B), providing metal base 120 that includes surfaces 122 and 124, central portion 126, slots 128, recessed portions 132 and 134, non-recessed portions 136 and leads 138 (Specification, page 9, lines 8-17 and Figs. 2A and 2B), forming metal traces 144 on metal base 120, where conductive traces 150 include leads 138 and metal traces 144 (Specification, page 11, lines 6-11 and Figs. 3A and 3B), forming transparent adhesive 154 on metal base 120 and metal traces 144 (Specification, page 12, lines 21-22 and Figs. 4A and 4B), mechanically attaching chip 110 to metal base 120 using transparent adhesive 154 (Specification, page 13, lines 5-6 and Figs. 5A and 5B), forming encapsulant 156 on chip 110 and metal base 120, where encapsulant 156 includes bottom surface 160, peripheral side surfaces 162, top surface 164 and peripheral

portion 166 (Specification, page 14, lines 3-4 and page 14, line 30 to page 15, line 1 and Figs. 6A and 6B), removing encapsulant 156 from laterally extending portions of slots 128 (Specification, page 15, lines 22-23 and Figs. 7A and 7B), forming protective coating 170 on metal base 120 outside encapsulant 156 (Specification, page 16, lines 9-10 and Figs. 8A and 8B), removing central portion 126 of metal base 120, thereby exposing metal traces 144 and transparent adhesive 154 (Specification, page 17, lines 7-8 and 12-13 and Figs. 9A and 9B), forming openings 176 in transparent adhesive 154 that expose pads 116 (Specification, page 18, lines 7-9 and Figs. 10A and 10B), forming connection joints 180 in openings 176 that contact and electrically connect pads 116 and metal traces 144 (Specification, page 18, line 28 to page 19, line 2 and Figs. 11A and 11B), forming transparent base 182 on the structure, where encapsulant 156 and transparent base 182 in combination form insulative housing 184 that surrounds and encapsulates chip 110 (Specification, page 20, lines 3-4 and 20-21 and Figs. 12A and 12B), singulating optoelectronic device 186 from the lead frame (Specification, page 21, lines 1-2 and 6-7 and Figs. 13A and 13B), and bending leads 138 (Specification, page 21, lines 18-20 and Figs. 14A and 14B).

Optoelectronic device 186 includes chip 110, conductive traces 150, transparent adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from and extends through a side surface 162 of insulative housing 184, and a metal trace 144 within insulative housing 184 that contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 164 and bottom surface 160. Furthermore, light sensitive cell 115 is protected by and exposed to incident light from the external environment by transparent adhesive 154 and transparent base 182. (Specification, page 21, lines 8-17.)

VI. ISSUES[1]

The issues on appeal are as follows:

1. Whether claim 76 is indefinite under 35 U.S.C. § 112, second paragraph;

2. Whether claims 1-10, 31-40, 91-93, 95-98, 100, 111-113, 115-118 and 120 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* (U.S. Patent No. 5,405,809) in view of *Fjelstad* (U.S. Patent No. 6,001,671);

3. Whether claims 11-20, 61-63, 65, 71-73, 75-78 and 80 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad;*

4. Whether claims 21-30, 141-143, 145-148 and 150 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad;*

5. Whether claims 41-51, 53-55 and 58-60 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Glenn et al.* (U.S. Patent No. 6,281,568);

6. Whether claims 52, 56 and 57 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad;*

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[1] Claims 1-40, 61-63, 65, 71-73, 75-78, 80, 91-93, 95-98, 100, 111-113, 115-118, 120, 141-143, 145-148 and 150 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad* at Section 9 in the outstanding Office Action dated July 31, 2003. Section 9 sets forth separate basis for rejection for independent claims 1, 11, 21, 31, 61, 71, 76, 91, 96, 111, 116, 141 and 146. Thus, the Examiner has set forth separate grounds of rejection for claims 1, 11, 21, 31, 61, 71, 76, 91, 96, 111, 116, 141 and 146 that constitute separate issues for appeal.

Claims 1, 31, 91, 96, 111 and 116 are sufficiently similar that they have been consolidated into the second issue for appeal, claims 11, 61, 71 and 76 are sufficiently similar that they have been consolidated into the third issue for appeal, and claims 21, 141 and 146 are sufficiently similar that they have been consolidated into the fourth issue for appeal.

Claims 64, 66-70, 74, 79, 94, 99, 114, 119, 144 and 149 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al* at Section 12 in the outstanding Office Action dated July 31, 2003. Section 12 sets forth separate basis for rejection for independent claim 66. Thus, the Examiner has set forth separate grounds of rejection for claim 66 that constitutes a separate issue for appeal.

Claims 64, 74 and 79 depend from independent claims 61, 71 and 76, respectively, and therefore form the seventh issue for appeal. Claims 94, 99, 114 and 119 depend from independent claims 91, 96, 111 and 116, respectively, and therefore form the eighth issue for appeal. Claims 144 and 149 depend from independent claims 141 and 146, respectively, and therefore form the ninth issue for appeal. Claim 66 forms the tenth issue for appeal.

7. Whether claims 64, 74 and 79 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.*;

8. Whether claims 94, 99, 114 and 119 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.*;

9. Whether claims 144 and 149 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.*;

10. Whether claims 66-70 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.*;

11. Whether claims 81-83, 85-88 and 90 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* (U.S. Patent No. 6,025,650);

12. Whether claims 84 and 89 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Fjelstad, Tsuji et al.* and *Glenn et al.*;

13 Whether claims 101-103, 105-108, 110, 121-123, 125-128, 130-133, 135-138 and 140 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Tsuji et al.*; and

14. Whether claims 104, 109, 124, 134 and 139 are unpatentable under 35 U.S.C. § 103(a) over *Nakamura et al.* in view of *Tsuji et al.* and *Glenn et al.*

VII. GROUPING OF CLAIMS

For the first issue on appeal, claim 76 is the sole claim.

For the second issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 1-5, 7-8, 10, 31-32, 34-37, 40, 91-92, 95-97 and 100, (ii) claims 6 and 33, (iii) claims 9 and 39, (iv) claim 38, (v) claims 93 and 98, (vi) claims 111-112, 115-117 and 120, and (vii) claims 113 and 118.

For the third issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 11-13, 15-18, 20, 61-62, 65, 71-72 and 75, (ii) claims 14, 63 and 73, (iii) claim 19, (iv) claims 76-77 and 80, and (v) claim 78.

For the fourth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 21-23, 25-30, 141-142 and 145, (ii) claim 24, (iii) claim 143, (iv) claims 146-147 and 150, and (v) claim 148.

For the fifth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 41-47, 50-51, 54-55 and 60, (ii) claims 48 and 58, (iii) claims 49 and 59, and (iv) claim 53.

For the sixth issue on appeal, the claims stand and fall together.

For the seventh issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 64 and 74, and (ii) claim 79.

For the eighth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 94 and 99, and (ii) claims 114 and 119.

For the ninth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claim 144, and (ii) claim 149.

For the tenth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 66-67 and 69-70, and (ii) claim 68.

For the eleventh issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 81-82, 85-87 and 90, and (ii) claims 83 and 88.

For the twelfth issue on appeal, the claims stand and fall together.

For the thirteenth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 101-102, 105-107, 110, 121-122, 125-127, 130-132, 135-137 and 140, and (ii) claims 103, 108, 123, 128, 133 and 138.

For the fourteenth issue on appeal, the claims stand and fall together.

VIII. ARGUMENTS

1. Section 112, Second Paragraph Rejection – Claim 76

Claim 76 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In sustaining this rejection, the Examiner asserts "In claim 76, line 3 from the bottom, the term 'the planar metal trace contacts' lacks antecedent basis." This is clearly erroneous.

Claim 76 recites "a conductive trace that includes a planar metal trace" at line 9, and "the planar metal trace contacts and is not integral with the lead" at lines 11-12. Thus, "a planar metal trace" at line 9 provides antecedent basis for "the planar metal trace" at line 11 (line 3 from the bottom).

2. Section 103 Rejections – Claims 1-10, 31-40, 91-93, 95-98, 100, 111-113, 115-118 and 120

Claims 1-10, 31-40, 91-93, 95-98, 100, 111-113, 115-118 and 120 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* (U.S. Patent No. 5,405,809) in view of *Fjelstad* (U.S. Patent No. 6,001,671).

Nakamura et al.

Nakamura et al. discloses an image sensor device that includes light-transmitting substrate 21, circuit conductor layer 22, plated metal layer 23, metal bump 24, image sensor chip 26, resin coating 27 and transparent resin 28. Image sensor chip 26 includes electrode 25 and light-sensitive element 29.

Metal bump 24 is a metal such as Au that is formed on electrode 25 by plating or ball bonding, and then image sensor chip 26 is cut out from a silicon wafer.

Circuit conductor layer 22 is a metal such as Cu or Al that is formed on light-transmitting substrate 21. For instance, circuit conductor layer 22 may be formed by depositing a metal layer

on light-transmitting substrate 21 by sputtering, vapor deposition and the like and then patterning the metal layer using photolithography. Alternatively, circuit conductive layer 22 may be formed by attaching a flexible printed wiring board to light-transmitting substrate 21 or by thick-film printing.

Plated metal layer 23 is then formed on a prescribed portion of circuit conductor layer 22.

Transparent resin 28 is then applied to a prescribed portion of light-transmitting substrate 21, and then image sensor chip 26 is disposed face-down on transparent resin 28 so that plated metal layer 23 abuts electrode 25. While image sensor chip 26 is pressed onto light-transmitting substrate 21, transparent resin 28 is irradiated with ultra violet rays through light-transmitting substrate 21 and partially cured.

The structure is then placed in an oven that melts plated metal layer 23 and further cures transparent resin 28. Plated metal layer 23 melts and recoagulates so that alloy layers are formed in abutting portions between circuit conductor layer 22 and plated metal layer 23, and in abutting portions between plated metal layer 23 and metal bump 24.

Finally, resin coating 27 such as silicon is dispensed on light-transmitting substrate 21 and image sensor chip 26.

Nakamura et al. emphasizes the importance of fully curing transparent resin 28 to provide a strong physical connection between light-transmitting substrate 21 and image sensor chip 26 so that the package is reliable and has good physical endurance:

> As is described above, in the first conventional method, the photo-curable insulating resin is cured by being irradiated with ultra violet rays through the transparent substrate. Therefore, a portion of the photo-curable insulating resin which is shaded by the circuit conductor layer formed on the transparent substrate may not be sufficiently irradiated with the ultra violet rays, and therefore may not be cured completely. In such cases, since the photocurable insulating resin is not completely cured, the physical connection between the semiconductor chip and the substrate is insufficient, causing the device to have poorer physical endurance. (Col. 2, lines 10-21.) (Emphasis added.)

> Moreover, the semiconductor device and the image sensor device each can be firmly mounted on a light-transmitting substrate, since a photo-thermal cross-linkable insulating resin included therein is completely cured through first and second curing steps, greatly improving the mounting yield of the devices. (Col. 5, lines 41-47.) (Col. 12, lines 55-61.) (Emphasis added.)
>
> Thus, the invention described herein makes possible the advantages of (1) providing a semiconductor device and an image sensor having high reliability, in which an insulating resin is completely cured and electrodes of a semiconductor chip have a firm electrical connection with a circuit conductor layer formed on a substrate, and (2) providing methods for producing such a semiconductor device and an image sensor device. (Col. 5, lines 51-59.) (Emphasis added.)

Accordingly, light-transmitting substrate 21 is an essential, permanent part of the image sensor device, and image sensor chip 26 is firmly mounted on light-transmitting substrate 21 by transparent resin 28 to assure a high reliability device with good physical endurance.

Fjelstad

Fjelstad discloses manufacturing a semiconductor package using a sacrificial layer that is removed so that when a heat sink is attached there is a more direct thermal path to draw heat away from the chip.

In an embodiment shown in Figures 1A-1G-1, sacrificial layer 100 comprised of aluminum is provided (Fig. 1A), pad 110 is formed on sacrificial layer 100 by electroplating (Fig. 1B), chip 120 that includes contact bearing face surface 121 and back surface 122 (mislabeled) is back bonded to sacrificial layer 100 by thermally conductive die attach adhesive 135 such that face surface 121 of chip 120 faces away from sacrificial layer 100 (Fig. 1C), the contact of chip 120 is electrically connected to pad 110 by wirebonded connection 130 (Fig. 1D-1), pad 110, chip 120 and wirebonded connection 130 are encapsulated by encapsulant 140 (Fig. 1E), sacrificial layer 100 is removed by etching to expose pad 110 and provide a direct thermal path to chip 120 through die attach adhesive 135 (Fig. 1F), and the individual packaged chips are separated from one another (Figure 1G-1).

In an alternative embodiment shown in Figures 5A-5H, sacrificial layer 200 is provided (Fig. 5A), photo-imageable dielectric layer 204 with aperture 205 is deposited on sacrificial layer 200 and cavity 203 is formed in sacrificial layer 200 beneath aperture 205 by etching (Fig. 5B), pad 210 with post pad 211 and bump flanges 212 and 213 is formed in cavity 203 by electroplating (Fig. 5C), photo-imageable dielectric layer 204 is removed and then chip 220 with contact bearing face surface 221 and back surface 222 is back bonded to sacrificial layer 200 by thermally conductive die attach adhesive 235 such that face surface 221 of chip 220 faces away from sacrificial layer 200 (Fig. 5D), the contact of chip 220 is electrically connected to pad 210 by wirebonded connection 230 (Fig. 5E), pad 210, chip 220 and wirebonded connection 230 are encapsulated by encapsulant 240 (Fig. 5F), sacrificial layer 200 is removed by etching to expose pad 210 and provide a direct thermal path to chip 220 through die attach adhesive 235 (Fig. 5G), and the individual packaged chips are separated from one another (Fig. 5H).

Claims 1-5, 7-8, 10, 31-32, 34-37, 40, 91-92, 95-97 and 100 (Group I)

Claim 1 recites "the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge and is exposed." Claims 31, 91 and 96 recite similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Light-transmitting substrate 21 is not located within a peripheral ledge of resin coating 27, and transparent resin 28 is not exposed. *Fjelstad* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly technique in *Fjelstad*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . an insulative housing (27 and 28).
>
> Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of

> ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. As best Applicant can tell, the Examiner is proposing to use light-transmitting substrate 21 in *Nakamura et al.* like sacrificial layer 200 in *Fjelstad* such that light-transmitting substrate 21 is removed from the image sensor device after resin coating 27 is formed. However, since the insulative housing is described both as resin coating 27 and transparent resin 28 and as die attach adhesive 235 and encapsulant 240, it is unclear whether encapsulant 240 replaces resin coating 27, and whether die attach adhesive 235 replaces transparent resin 28. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

Moreover, the proposed modification is not taught or suggested by *Fjelstad*, has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose.

Fjelstad fails to teach or suggest the proposed modification. *Fjelstad* removes sacrificial layer 200 from the back side of a wire bonded chip but fails to teach or suggest removing sacrificial layer 200 from the front side of flip-chip. *Fjelstad* removes sacrificial layer 200 to expose an unexposed conductor but fails to teach or suggest removing sacrificial layer 200 to expose an exposed conductor. *Fjelstad* removes sacrificial layer 200 to provide a direct thermal path to the back side of a chip but fails to teach or suggest removing sacrificial layer 200 to provide a direct thermal path to the front side of a chip that already contains a direct thermal path to the back side. *Fjelstad* removes sacrificial layer 200 to position a heat sink over the back side of a chip but fails to teach or suggest removing sacrificial layer 200 to position a heat sink over the front side of an optoelectronic chip.

Furthermore, since light-transmitting substrate 21 is an essential, permanent part of the image sensor device, the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose, and therefore there is no teaching, suggestion or motivation for this modification.

The Examiner attempts to cure this fundamental deficiency by asserting that *Fjelstad* supplies the necessary motivation by providing a direct thermal path to facilitate the removal of heat from the packaged chip. However, *Fjelstad* removes sacrificial layer 200 to provide a direct thermal path to the back side of a wire bonded chip rather than the front side of a flip-chip, whereas *Nakamura et al.* already provides a direct thermal path to the back side of image sensor chip 26 through resin coating 27. Furthermore, although one skilled in the art might be motivated to position a heat sink over the back side of a chip to increase heat removal, one skilled in the art would not be motivated to position a heat sink over the front side of an optoelectronic chip since this would screen the light sensitive cell. Moreover, although one skilled in the art might be motivated to remove a sacrificial layer to facilitate heat removal from a packaged chip, one skilled in the art would not be motivated to remove an essential, permanent part of a package (like light-transmitting substrate 21) to facilitate heat removal since this would degrade or destroy the device. *Nakamura et al.* emphasizes the importance of fully curing transparent resin 28 to provide a strong physical connection between light-transmitting substrate 21 and image sensor chip 26 so that the package is reliable and has good physical endurance. Thus, light-transmitting substrate 21 is an essential, permanent part of the image sensor device. Since removing light-transmitting substrate 21 would render *Nakamura et al.* unsatisfactory for its intended purpose, there is no motivation to do so.

Therefore, the proposed modification is clearly erroneous.

Claims 6 and 33 (Group II)

Claim 6 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 6 recites "the second housing portion is recessed relative to the peripheral ledge." Claim 33 recites similar limitations. *Nakamura et al.* fails to teach or suggest that transparent resin 28 is recessed relative to a peripheral ledge of resin coating 27. Instead, transparent resin 28 and resin coating 27 extend to light-transmitting substrate 21. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses in Fig. 2 the second housing portion being recessed relative to the peripheral ledge." This is clearly erroneous.

Claims 9 and 39 (Group III)

Claim 9 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 9 recites "the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion." Claim 39 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach if light-transmitting substrate 21 is removed. Instead, circuit conductor layer 22, plated metal layer 23 and metal bump 24 in combination provide an electrical conductor that extends through opposing surfaces of transparent resin 28. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion." This is clearly erroneous under the proposed modification.

Claim 38 (Group IV)

Claim 38 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 38 recites "the device is devoid of an electrical conductor that extends through the top or bottom surfaces." *Nakamura et al.* fails to teach or suggest this approach if light-transmitting substrate 21 is removed. Instead, circuit conductor layer 22, plated metal layer 23 and metal bump 24 in combination provide an electrical conductor that extends through transparent resin 28 at the top surface. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces." This is clearly erroneous under the proposed modification.

Claims 93 and 98 (Group V)

Claim 93 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 93 recites "the conductive trace extends through an opening in one of the peripheral side surfaces [of the first housing portion]." Claim 98 recites similar limitations. *Nakamura et al.* fails to teach or suggest that circuit conductor layer 22 extends through an opening in resin coating 27. In sustaining this rejection, the Examiner asserts that "Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces." This is clearly erroneous since it ignores the claim limitation that the first housing portion provides the peripheral side surfaces. Moreover, the Examiner admits that "Nakamura et al. does not disclose a conductive trace that extends through an opening in the first housing portion" in the rejection of claim 11.

Claims 111-112, 115-117 and 120 (Group VI)

Claim 111 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 111 recites "the conductive trace . . . is spaced from the top surface." Claim 116 recites similar limitations. *Nakamura et al.* fails to teach or suggest that circuit conductor layer 22 is spaced from the top surface if light-transmitting substrate 21 is removed. Instead, the top surface would include circuit conductor layer 22 and transparent resin 28. In sustaining this rejection, the Examiner asserts that "a conductive trace (22) . . . is spaced from the top surface." This is clearly erroneous under the proposed modification.

Claims 113 and 118 (Group VII)

Claim 113 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group VI claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 113 recites "the conductive trace extends through an opening in one of the peripheral side surfaces [of the first housing portion]." Claim 118 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 93.

3. Section 103 Rejections – Claims 11-20, 61-63, 65, 71-73, 75-78 and 80

Claims 11-20, 61-63, 65, 71-73, 75-78 and 80 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad.*

Claims 11-13, 15-18, 20, 61-62, 65, 71-72 and 75 (Group I)

Claim 11 recites "a conductive trace that extends through an opening in the first housing portion." Claims 61 and 71 recite similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Circuit conductor layer 22 does not extend through an opening in resin coating 27. *Fjelstad* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly technique in *Fjelstad*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . an insulative housing (27 and 28) . . . and a conductive trace (22).
>
> Nakamura et al. does not disclose a conductive trace that extends through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5H a conductive trace (213) that extends through an opening (at the place of 235) in a first housing portion (240). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace to be extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct contact (column 2, lines 59 ~ 60).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. It is unclear whether encapsulant 240 replaces resin coating 27, and whether die attach adhesive 235 replaces transparent resin 28, as mentioned above for claim 1. It is also unclear whether pad 210 replaces circuit conductor layer 22.

Fjelstad fails to teach or suggest the proposed modification, as explained above for claim 1. Furthermore, *Fjelstad* electroplates pad 210 on aluminum sacrificial layer 200 but fails to teach or suggest electroplating pad 210 on an insulative substrate (like light-transmitting substrate 21). Aluminum sacrificial layer 200 cannot replace light-transmitting substrate 21 since aluminum sacrificial layer 200 would reflect rather than transmit the ultra violet rays that pass through light-transmitting substrate 21 and partially cure transparent resin 28.

Moreover, the proposed modification has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose, as mentioned above for claim 1.

The Examiner attempts to cure this fundamental deficiency by asserting that *Fjelstad* supplies the necessary motivation by providing a direct contact. However, *Fjelstad* removes

sacrificial layer 200 to expose an unexposed electrical conductor, whereas *Nakamura et al.* already exposes circuit conductor layer 22.

Therefore, the proposed modification is clearly erroneous.

Claims 14, 63 and 73 (Group II)

Claim 14 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 14 recites "the second housing portion is recessed relative to the peripheral ledge." Claims 63 and 73 recite similar limitations. *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

Claim 19 (Group III)

Claim 19 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 19 recites "the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion." *Nakamura et al.* fails to teach or suggest this approach under the proposed modification, as mentioned above for claim 9.

Claims 76-77 and 80 (Group IV)

Claim 76 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 76 recites "a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion . . . and the planar metal trace contacts and is not integral with the lead [and] extends across one of the side surfaces [of the chip]." *Nakamura et al.* fails to teach or suggest this approach since plated metal layer 23 does not extend across a side surface of image sensor chip 26. *Fjelstad* fails to cure this deficiency since wirebonded connection 230 is not planar. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses . . . a conductive trace (22 and 23) that includes a lead (22) and a planar metal traces (23), wherein the lead extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing." This is clearly erroneous. Circuit conductor layer 22 does not extend through an opening in resin coating 27, as explained above for claim 93. In addition, plated metal layer 23 does not extend across a side surface of image sensor chip 26.

Claim 78 (Group V)

Claim 78 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group IV claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 78 recites "the second housing portion is located within and recessed relative to the peripheral ledge." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

4. Section 103 Rejections – Claims 21-30, 141-143, 145-148 and 150

Claims 21-30, 141-143, 145-148 and 150 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad.*

Claims 21-23, 25-30, 141-142 and 145 (Group I)

Claim 21 recites "an insulative housing that includes a top surface, a bottom surface and uncurved peripheral side surfaces between the top and bottom surfaces." Claim 141 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Resin coating 27 has curved peripheral side surfaces. *Fjelstad* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly technique in *Fjelstad*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . an insulative housing (27 and 28).
>
> Nakamura et al. does not disclose the design of the first insulative housing portion that has uncurved peripheral side surfaces between the top and bottom surfaces. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of the first insulative housing portion (240) that has uncurved peripheral sidewalls between top and bottom surfaces. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the first insulative housing portion to have uncurved peripheral side surfaces between the top and bottom surfaces as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of reducing a size of the semiconductor package.

The rejection is flawed for several reasons.

The proposed modification apparently uses encapsulant 240 in *Fjelstad* as resin coating 27 in *Nakamura et al.* However, the proposed modification is vague and confusing as to which process steps in Figs. 5F-5H of *Fjelstad* are being applied to *Nakamura et al.* It is also unclear whether encapsulant 240 extends outside light-transmitting substrate 21 (like encapsulant 240 extends outside die attach adhesive 235) or does not (like resin coating 27).

Fjelstad fails to teach or suggest the proposed modification. *Fjelstad* forms encapsulant 240 on a sacrificial layer and then removes the sacrificial layer but fails to teach or suggest forming encapsulant 240 on a permanent base (like light-transmitting substrate 21). *Fjelstad* forms encapsulant 240 over multiple chips and then slices encapsulant 240 to separate the chips but fails to teach of suggest forming encapsulant 240 over a single chip (like image sensor chip 26).

Encapsulant 240 is sliced in Fig. 5H to form uncurved peripheral sidewalls outside pads 210 so that the individual packaged chips are diced or separated from one another. Those skilled in the art would recognize that encapsulant 240 is sliced by a cutting tool such as a saw or excise blade.

If encapsulant 240 surrounded circuit conductor layer 22 (as taught by *Fjelstad*) and the cutting tool sliced encapsulant 240 outside circuit conductor layer 22 to separate individual image sensor devices (as taught by *Fjelstad*) then circuit conductor layer 22 would not be exposed, thereby rendering *Nakamura et al.* unsatisfactory for its intended purpose.

If encapsulant 240 surrounded circuit conductor layer 22 (as taught by *Fjelstad*) and the cutting tool sliced encapsulant 240 within circuit conductor layer 22 (not taught by *Fjelstad*) and sliced light-transmitting substrate 21 and circuit conductor layer 22 (not taught by *Fjelstad*) then circuit conductor layer 22 would be exposed only at a narrow distal end aligned with a peripheral side surface of encapsulant 240, thereby rendering *Nakamura et al.* unsatisfactory for its intended purpose.

If encapsulant 240 did not surround circuit conductor layer 22 (not taught by *Fjelstad*) and the cutting tool sliced encapsulant 240 within circuit conductor layer 22 (not taught by *Fjelstad*) and attempted not to slice through circuit conductor layer 22 (not taught by *Fjelstad*) then the cutting tool would likely damage circuit conductive layer 22, thereby rendering *Nakamura et al.* unsatisfactory for its intended purpose.

Therefore, the proposed modification has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose.

The Examiner attempts to cure this fundamental deficiency by asserting that *Fjelstad* supplies the necessary motivation to reduce the size of the semiconductor package. However, *Fjelstad* extends encapsulant 240 outside the peripheries of pad 210 and die attach adhesive 235, whereas *Nakamura et al.* confines resin coating 27 within the peripheries of light-transmitting substrate 21 and circuit conductor layer 22.

Therefore, the proposed modification is clearly erroneous.

Claim 24 (Group II)

Claim 24 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 24 recites "the second housing portion is located within and recessed relative to the peripheral ledge." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

Claim 143 (Group III)

Claim 143 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 143 recites "the conductive trace extends through an opening in one of the peripheral side surfaces [of the first housing portion]." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 93.

Claims 146, 147 and 150 (Group IV)

Claim 146 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad*

on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 146 recites "the first housing portion . . . includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces [and] a peripheral ledge at the top surface . . . [and] the second housing portion extends into the peripheral ledge . . . [and] is exposed at the top surface." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 1.

Claim 148 (Group V)

Claim 148 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for the Group IV claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad.*

Claim 148 recites "the conductive trace extends through an opening in one of the peripheral side surfaces [of the first housing portion]." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 93.

5. Section 103 Rejections – Claims 41-51, 53-55 and 58-60

Claims 41-51, 53-55 and 58-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* (U.S. Patent No. 6,281,568).

Glenn et al.

Glenn et al. discloses a semiconductor package in which an encapsulant prevents the die pad and the lead from being pulled vertically from the package.

Leadframe 20 includes tie bar 21, die pad 22, connector 28, dam bar 29 and lead 30 (Fig. 2). Die pad 22 includes first upper surface 23, second (unrecessed) surface 24, third (recessed) surface 25 and side surfaces 26 and 27 (Fig. 3). Lead 30 includes first surface 31, second

(unrecessed) surface 32, third (recessed) surface 33 and lateral sides 37 (Fig. 3). Lower surfaces 25 and 33 of die pad 22 and lead 30 are vertically recessed a distance H1.

Integrated circuit die 52 that includes bond pad 53 is attached to die pad 22 using a die attach epoxy, then lead 30 is electrically connected to pad 53 by bond wire 54, then package body 51 (the encapsulant material) covers die 52, bond wire 54, surfaces 23, 25, 26 and 27 of die pad 22 and surfaces 31, 33 and 37 of lead 30 without covering surface 24 of die pad 22 or surface 32 of lead 30 (Fig. 5). Package body 51 fills beneath surface 25 of die pad 22 and beneath surface 33 of lead 30 to prevent die pad 22 and lead 30 from being pulled vertically from the package. Thereafter, connector 28 and lead 30 are severed from dam bar 29 to form the completed package.

Package 50 includes tapered side surfaces 55 and lower surface 56. Lead 30 includes severed end portion 35 that laterally extends beyond side surface 55 and is bent upwards at an oblique angle to lower surface 56. Lower surface 56 includes die pad 22, lead 30 and package body 51.

Claims 41-47, 50-51, 54-55 and 60 (Group I)

Claim 41 recites "a conductive trace that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the conductive trace includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and the top surface." Claim 51 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Circuit conductor layer 22 does not include recessed and non-recessed portions. *Glenn et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly technique in *Glenn et al.*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . an insulative housing (27 and 28) . . . and a conductive trace (22).
>
> Nakamura et al. does not disclose the conductive trace including a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and the top surface. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) that extends into an insulative housing (51) and is spaced from a top and bottom surfaces and a non-recessed portion (32) that extends outside the insulative housing and is adjacent to the recessed portion at the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

The rejection is flawed for several reasons.

The proposed modification apparently uses lead 30 in *Glenn et al.* as circuit conductor layer 22 in *Nakamura et al.*

The proposed modification is not taught or suggested by *Glenn et al.*, has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose.

Glenn et al. fails to teach or suggest the proposed modification. *Glenn et al.* provides a leadframe with a die pad and a lead, mounts a chip on the die pad, wire bonds the chip to the lead and then forms a package body that extends beneath a recessed portion of the lead, but fails to teach or suggest this approach with a flip-chip. *Glenn et al.* provides a leadframe with a die pad and a lead but fails to teach or suggest a leadframe without a die pad. *Glenn et al.* wire bonds the recessed portion of the lead but fails to teach or suggest mounting the chip on the recessed portion of the lead. *Glenn et al.* spaces the lead from a die attach epoxy but fails to teach or

suggest contacting the lead to a die attach epoxy. *Glenn et al.* fills the package body into the entire recessed portion of the lead but fails to teach or suggest partially filling another material into the recessed portion of the lead. *Glenn et al.* positions the lead outside the periphery of the chip but fails to teach or suggest extending the lead into the periphery of the chip. *Glenn et al.* extends the lead to a major surface of the package but fails to teach or suggest spacing the lead from a major surface of the package.

The Examiner attempts to cure this fundamental deficiency by asserting that *Glenn et al.* supplies the necessary motivation to prevent the lead from being pulled vertically from the package. However, *Glenn et al.* fills the package body into the recess of a lead that has no back side support, whereas *Nakamura et al.* already provides back side support for circuit conductor layer 22 with light-transmitting substrate 21. In fact, the entire back side of circuit conductor layer 22 is mounted on and supported by light-transmitting substrate 21. Thus, the vertical lead pull problem in *Glenn et al.* does not exist in *Nakamura et al.*, and the motivation set forth by the Examiner does not exist.

Moreover, since light-transmitting substrate 21 and circuit conductor layer 22 are attached to one another (rather than integral with one another like die pad 22 and lead 30), if circuit conductor layer 22 included recessed portion 33 beneath image sensor chip 26 then mounting image sensor chip 26 on the recessed portion of the lead would apply pressure that could detach or separate the non-recessed portion of the lead from light-transmitting substrate 21. *Nakamura et al.* emphasizes the importance of a high reliability package, and this modification is inconsistent with this objective.

Moreover, lead 30 would need to be severed from dam bar 29 after forming resin coating 27, thereby laterally protruding lead 30 outside light-transmitting substrate 21 and increasing the size of the image sensor device.

Therefore, the proposed modification is clearly erroneous.

Claims 48 and 58 (Group II)

Claim 48 distinguishes over *Nakamura et al.* in view of *Glenn et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Glenn et al.* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Glenn et al.*

Claim 48 recites "the device is devoid of an electrical conductor that extends through the top or bottom surfaces." Claim 58 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach under the proposed modification, as mentioned above for claim 38.

Claims 49 and 59 (Group III)

Claim 49 distinguishes over *Nakamura et al.* in view of *Glenn et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Glenn et al.* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Glenn et al.*

Claim 49 recites "the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion." Claim 59 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach under the proposed modification, as mentioned above for claim 9.

Claim 53 (Group IV)

Claim 53 distinguishes over *Nakamura et al.* in view of *Glenn et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Glenn et al.* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Glenn et al.*

Claim 53 recites "the second housing portion is located within and recessed relative to the peripheral ledge." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

6. Section 103 Rejections – Claims 52, 56 and 57

Claims 52, 56 and 57 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad.*

Claims 52, 56 and 57 distinguish over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad* for the reasons set forth above for claim 41.

7. Section 103 Rejections – Claims 64, 74 and 79

Claims 64, 74 and 79 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad.*

Claims 64 and 74 (Group I)

Claims 64 and 74 distinguish over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for claim 11.

Claim 64 recites "the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion." Claim 74 recites similar limitations.

Nakamura et al. in view of *Fjelstad* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 41.

In sustaining this rejection, the Examiner asserts that *Nakamura et al.* as modified by *Fjelstad* can be further modified by *Glenn et al.* to meet the claim limitations.

The proposed modification is vague and confusing as to how *Nakamura et al.* is modified by *Fjelstad*, as mentioned above for claim 11.

The proposed modification is also vague and confusing as to how *Nakamura et al.* as modified by *Fjelstad* would be further modified by *Glenn et al.* Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

As best Applicant can tell, the Examiner is proposing to use lead 30 in *Glenn et al.* as pad 210 in *Fjelstad*. However, pad 210 is formed additively on sacrificial layer 200 by electroplating whereas lead 30 is recessed subtractively by chemical etching according to a resist pattern on leadframe 20. If lead 30 was formed on sacrificial layer 200 by electroplating then sacrificial layer 200 would prevent forming a resist pattern on the lower surface of lead 30, and thus recessed surface 33 could not be formed.

The Examiner attempts to cure this fundamental deficiency by asserting that *Glenn et al.* supplies the necessary motivation to prevent the lead from being pulled vertically from the package. However, the vertical lead pull problem in *Glenn et al.* does not exist in *Nakamura et al.*, as mentioned above for claim 41. Moreover, *Fjelstad* already forms pad 210 with bump flange 212 so that encapsulant 240 provides back side support for pad 210. Thus, the vertical lead pull problem in *Glenn et al.* does not exist in *Fjelstad*.

Therefore, the proposed modification is clearly erroneous.

Claim 79 (Group II)

Claim 79 distinguishes over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.* for the reasons set forth above for the Group I claims and claim 76.

8. Section 103 Rejections – Claims 94, 99, 114 and 119

Claims 94, 99, 114 and 119 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad.*

Claims 94 and 99 (Group I)

Claims 94 and 99 distinguish over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for claim 1.

Claims 94 and 99 recite similar limitations as claim 64. *Nakamura et al.* in view of *Fjelstad* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 64.

In sustaining this rejection, the Examiner asserts that *Nakamura et al.* as modified by *Fjelstad* can be further modified by *Glenn et al.* to meet the claim limitations. However, the proposed modification is vague and confusing, *Glenn et al.* fails to teach or suggest using lead 30 as pad 210 in *Fjelstad*, and there is no motivation to do so, as mentioned above for claim 64.

Claims 114 and 119 (Group II)

Claims 114 and 119 distinguish over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.* for the reasons set forth above for the Group I claims and claim 111.

9. Section 103 Rejections – Claims 144 and 149

Claims 144 and 149 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad.*

Claim 144 (Group I)

Claim 144 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for claim 21.

Claim 144 recites similar limitations as claim 64. *Nakamura et al.* in view of *Fjelstad* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 64.

In sustaining this rejection, the Examiner asserts that *Nakamura et al.* as modified by *Fjelstad* can be further modified by *Glenn et al.* to meet the claim limitations. However, the proposed modification is vague and confusing, *Glenn et al.* fails to teach or suggest using lead 30 as pad 210 in *Fjelstad*, and there is no motivation to do so, as mentioned above for claim 64.

Claim 149 (Group II)

Claim 149 distinguishes over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.* for the reasons set forth above for the Group I claim and claim 146.

10. Section 103 Rejections – Claims 66-70

Claims 66-70 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Glenn et al.* and *Fjelstad.*

Claims 66-67 and 69-70 (Group I)

Claim 66 distinguishes over *Nakamura et al.* in view of *Fjelstad* for the reasons set forth above for claim 11.

Claim 66 recites "the conductive trace . . . is bent outside the insulative housing."

Nakamura et al. in view of *Fjelstad* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 64.

In sustaining this rejection, the Examiner asserts that *Nakamura et al.* as modified by *Fjelstad* can be further modified by *Glenn et al.* to meet the claim limitations. However, the proposed modification is vague and confusing, *Glenn et al.* fails to teach or suggest using lead 30 as pad 210 in *Fjelstad*, and there is no motivation to do so, as mentioned above for claim 64.

Claim 68 (Group II)

Claim 68 distinguishes over *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in

view of *Fjelstad* and *Glenn et al.* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad* and *Glenn et al.*

Claim 68 recites "the second housing portion is located within and recessed relative to the peripheral ledge." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

11. Section 103 Rejections – Claims 81-83, 85-88 and 90

Claims 81-83, 85-88 and 90 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* (U.S. Patent No. 6,025,650).

Tsuji et al.

Tsuji et al. discloses semiconductor device 21G in Figs. 18A and 18B. Semiconductor device 21G includes resin portion 23, frame terminal 27, pole terminal 28A, solder portion 29, semiconductor chip 41, adhesive 42, wire 43, first insulating layer 51a, second insulating layer 51b, pattern layer 52, third insulating layer 53 and outer terminal portion 67.

Semiconductor device 21G is manufactured by providing clad metal 60 with inner layer portion 61 and outer layer portions 62 and 63 (Fig. 19A), selectively etching outer layer portions 62 and 63 (Fig. 19B), and half-etching inner layer portion 61 using outer layer portions 62 and 63 as etch masks to form etching portions 64 and 65 in opposite sides of inner layer portion 61 and thin portion 66 between etching portions 64 and 65 (Fig. 19C). Pole terminal 28A includes outer layer portions 62 and 63 and inner layer portion 61 therebetween and is positioned between etching portions 64 and 65 and thin portions 66.

First insulating layer 51a is filled into etching portion 64 (Fig. 16A), second insulating layer 51b is formed on first insulating layer 51a and contains an opening that selectively exposes pole terminal 28A (Fig. 16B), pattern layer 52 is formed by aluminum vapor deposition, photo-etching and then plating on first insulating layer 51a and pole terminal 28A (Fig. 16C), and third insulating layer 53 is formed on second insulating layer 51b and pattern layer 52 (Fig. 16D).

Semiconductor chip 41 is mounted on third insulating layer 53 through adhesive 42, pad 41a of semiconductor chip 41 is electrically connected to pattern layer 52 by wire 43, and resin portion 23 seals semiconductor chip 41 (Fig. 20A), thin portion 66 is etched and removed (Fig. 20B), and solder portion 29 is provided on the pole terminal 28A (Fig. 20C).

Claims 81-82, 85-87 and 90 (Group I)

Claim 81 recites "a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first and second housing portions, extends across one of the side surfaces and does not extend outside the insulative housing." Claim 86 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach since plated metal layer 23 does not extend across a side surface of image sensor chip 26. *Fjelstad* fails to cure this deficiency since wirebonded connection 230 is not planar. *Tsuji et al.* fails to cure this deficiency since pattern layer 52 is not planar. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly techniques in *Fjelstad* and *Tsuji et al.*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . a conductive trace (22 and 23) that includes a lead (22) and a planar metal traces (23), wherein the lead extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing.
>
> Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed and a lead (213) extending through an opening (at the place of the 235) in a first housing portion (240).

> Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed and the conductive trace extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).
>
> Further, Nakamura et al., as modified, does not disclose the planar metal trace contacting the first and second housing portions. However, Tsuji et al. discloses in Fig. 18A a planar metal trace (52) contacting first (23) and second (53) housing portions. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the planar metal trace as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of coping with different sizes of semiconductor chips (column 2, lines 57 ~ 61).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing as to how *Nakamura et al.* is modified by *Fjelstad*, as mentioned above for claims 1 and 11.

The proposed modification is also vague and confusing as to how *Nakamura et al.* as modified by *Fjelstad* would be further modified by *Tsuji et al.* It is unclear whether patterned layer 52 is replacing circuit conductor layer 22, plated metal layer 23, metal bump 24, pad 210 or some combination thereof, or being added in some manner. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

The proposed modification is not taught or suggested by *Fjelstad*, has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose, as mentioned above for claims 1 and 11.

The proposed modification is not taught or suggested by *Tsuji et al.*, has no motivation and would render *Nakamura et al.* unsatisfactory for its intended purpose.

Tsuji et al. fails to teach or suggest the proposed modification. *Tsuji et al.* provides semiconductor device 21G as a wire bonded chip with back side lattice terminal poles that underlay the chip, but fails to teach or suggest this approach with a flip-chip.

The Examiner attempts to cure this fundamental deficiency by asserting that *Tsuji et al.* supplies the necessary motivation to cope with different sizes of semiconductor chips. However, *Tsuji et al.* discloses these advantages in the context of a wire bonded chip, whereas *Nakamura et al.* provides a flip-chip.

Moreover, even if the proposed modification was made (although there is no teaching, suggestion or motivation to do so), the proposed modification would not meet the claim limitations since pattern layer 52 is not planar. Instead, pattern layer 52 protrudes through an opening in second insulating layer 51b to contact pole terminal 28A.

Therefore, the proposed modification is clearly erroneous.

Claims 83 and 88 (Group II)

Claim 83 distinguishes over *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.*

Claim 83 recites "the second housing portion is located within and recessed relative to the peripheral ledge." Claim 88 recites similar limitations. *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 6.

12. Section 103 Rejections – Claims 84 and 89

Claims 84 and 89 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Fjelstad, Tsuji et al.* and *Glenn et al.*

Claims 84 and 89 distinguish over *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* for the reasons set forth above for claim 81.

Claims 84 and 89 recite similar limitations as claim 64. *Nakamura et al.* in view of *Fjelstad* and *Tsuji et al.* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 64.

13. Section 103 Rejections – Claims 101-103, 105-108, 110, 121-123, 125-128, 130-133, 135-138 and 140

Claims 101-103, 105-108, 110, 121-123, 125-128, 130-133, 135-138 and 140 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Tsuji et al.*

Tsuji et al.

Tsuji et al. discloses semiconductor device 90 in Figs. 26A and 26B. Semiconductor device 90 includes semiconductor chip 91, resin package 92, wire 93 and pole terminal 94. Semiconductor device 90 differs from a conventional quad flat package in that pole terminal 94 extends vertically from the resin package rather than outwardly from a periphery of the resin package to reduce package size.

Semiconductor device 90 is manufactured by providing metal plate 96 and resists 98a and 98b (Fig. 28A), and half-etching metal plate 96 using resists 98a and 98b as etch masks to form grooves 99 and 100 in opposite sides of metal plate 96, thin portion 101 outside grooves 99 and 100 and thin portion 102 between grooves 99 and 100 such that pole terminal 94 includes metal plate 96 between thin portions 101 and 102, and removing resists 98a and 98b (Fig. 28B).

Semiconductor chip 91 is mounted on thin portion 101 through pad material 95, semiconductor chip 91 is electrically connected to pole terminal 94 by wire 93 (Fig. 28C), the structure is placed in mold 105 (Fig. 28D), resin package 92 seals semiconductor chip 91 (Fig. 29A), and thin portions 101 and 102 are etched and removed and resin package 92 is cut (Fig. 29B).

As a variation, pad material 95 is removed, thereby exposing the bottom surface of semiconductor chip 91 (Fig. 30A).

Claims 101-102, 105-107, 110, 121-122, 125-127, 130-132, 135-137 and 140 (Group I)

Claim 101 recites "the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, and the top surface is exposed." Claims 106, 121, 126, 131 and 136 recite similar limitations. *Nakamura et al.* fails to teach or suggest this approach. Light-transmitting substrate 21 is not located within or recessed relative to a peripheral portion of resin coating 27, and transparent resin 28 is not recessed relative to a peripheral portion of resin coating 27 or exposed. *Tsuji et al.* fails to cure this deficiency since pad material 95 is not recessed relative to resin package 92. There is no teaching, suggestion or motivation to modify *Nakamura et al.* using the assembly technique in *Tsuji et al.*, particularly since the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Nakamura et al. discloses . . . an insulative housing (27 and 28).
>
> Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed at the top surface and the central portion of the top surface being recessed relative to the peripheral portion of the top surface. However, Tsuji et al. teaches in FIG. 26 an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a second housing portion (95) being exposed at the top surface and a central portion of the top surface being recessed relative to the peripheral portion of the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that

has the second housing portion being exposed at the top surface as taught by Tsuji. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. As best Applicant can tell, the Examiner is proposing to use light-transmitting substrate 21 in *Nakamura et al.* like thin portion 101 of metal plate 96 in *Tsuji et al.* such that light-transmitting substrate 21 is removed from the image sensor device after resin coating 27 is formed. However, since the insulative housing is described both as resin coating 27 and transparent resin 28 and as resin package 92 and pad material 95, it is unclear whether resin package 92 replaces resin coating 27, and whether pad material 95 replaces transparent resin 28. Furthermore, since col. 23, lines 33-34 pertains to Fig. 30A rather than Fig. 26A, it is unclear what device is referred to. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

Moreover, the proposed modification is not taught or suggested by *Tsuji et al.*, has no motivation, would render *Nakamura et al.* unsatisfactory for its intended purpose and fails to meet the claim limitations.

Tsuji et al. fails to teach or suggest the proposed modification. *Tsuji et al.* removes thin portion 101 of metal plate 96 from the back side of a wire bonded chip but fails to teach or suggest removing thin portion 101 of metal plate 96 from the front side of flip-chip. *Tsuji et al.* removes thin portion 101 of metal plate 96 to electrically isolate electrical conductors from one another but fails to teach or suggest removing thin portion 101 of metal plate 96 for electrical conductors that are already electrically isolated from one another. *Tsuji et al.* removes thin portion 101 of metal plate 96 to provide a thermal path to the back side of a chip but fails to teach or suggest removing thin portion 101 of metal plate 96 to provide a thermal path to the front side of a chip that already contains a thermal path to the back side or to the front side of an optoelectronic chip.

Furthermore, since light-transmitting substrate 21 is an essential, permanent part of the image sensor device, the proposed modification would render *Nakamura et al.* unsatisfactory for its intended purpose, and therefore there is no teaching, suggestion or motivation for this modification, as mentioned above for claim 1.

The Examiner attempts to cure this fundamental deficiency by asserting that *Tsuji et al.* supplies the necessary motivation by increasing reliability of the semiconductor package. However, one skilled in the art would not be motivated to remove an essential, permanent part of a package (like light-transmitting substrate 21) since this would degrade or destroy the device. *Nakamura et al.* emphasizes the importance of fully curing transparent resin 28 to provide a strong physical connection between light-transmitting substrate 21 and image sensor chip 26 so that the package is reliable and has good physical endurance. Thus, light-transmitting substrate 21 is an essential, permanent part of the image sensor device. Since removing light-transmitting substrate 21 would render *Nakamura et al.* unsatisfactory for its intended purpose, there is no motivation to do so.

Nakamura et al. teaches against removing light-transmitting substrate 21. Although the Examiner asserts that the proposed modification would increase reliability of the image sensor device, *Nakamura et al.* makes clear that the proposed modification would decrease reliability of the image sensor device.

Moreover, even if the proposed modification was made (although there is no teaching, suggestion or motivation to do so), the proposed modification would not meet the claim limitations since transparent resin 28 is not recessed relative to a peripheral portion of resin coating 27, as mentioned above for claim 6.

Therefore, the proposed modification is clearly erroneous.

Claims 103, 108, 123, 128, 133 and 138 (Group II)

Claim 103 distinguishes over *Nakamura et al.* in view of *Tsuji et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Nakamura et al.* in view of

Tsuji et al. on its own merits since it recites another limitation that is not disclosed by *Nakamura et al.* in view of *Tsuji et al.*

Claim 103 recites "the conductive trace extends through an opening in one of the peripheral side surfaces [of the first housing portion]." Claims 108, 123, 128, 133 and 138 recite similar limitations. *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 93.

14. Section 103 Rejections – Claims 104, 109, 124, 134 and 139

Claims 104, 109, 124, 134 and 139 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura et al.* in view of *Tsuji et al.* and *Glenn et al.*

Claims 104, 109, 124, 134 and 139 distinguish over *Nakamura et al.* in view of *Tsuji et al.* for the reasons set forth above for claim 101.

Claims 104, 109, 124, 134 and 139 recite similar limitations as claim 64. *Nakamura et al.* in view of *Tsuji et al.* fails to teach or suggest this approach, and *Glenn et al.* fails to cure this deficiency, as mentioned above for claim 64.

Conclusion

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

For the reasons given above, Applicant respectfully submits that claims 1-150 are in condition for allowance and respectfully requests that the outstanding rejections be overturned.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 18, 2003.

D Sigmond — 8/18/03

David M. Sigmond, Attorney for Applicant — Date of Signature

Respectfully submitted,

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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

2. The device of claim 1, wherein the first housing portion contacts four outer side surfaces of the chip.

3. The device of claim 1, wherein the first housing portion is spaced from the upper surface.

4. The device of claim 1, wherein the second housing portion contacts the conductive trace.

5. The device of claim 1, wherein the second housing portion is spaced from the lower surface.

6. The device of claim 1, wherein the second housing portion is recessed relative to the peripheral ledge.

7. The device of claim 1, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

8. The device of claim 1, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

9. The device of claim 1, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

10. The device of claim 1, wherein the device is devoid of wire bonds, TAB leads and solder joints.

11. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell and is spaced from the lower surface; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

12. The device of claim 11, wherein the second housing portion includes first and second opposing surfaces, the first surface contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

13. The device of claim 12, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

14. The device of claim 13, wherein the second housing portion is recessed relative to the peripheral ledge.

15. The device of claim 11, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

16. The device of claim 11, wherein the insulative housing consists of the first and second housing portions.

17. The device of claim 11, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

18. The device of claim 11, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

19. The device of claim 11, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

20. The device of claim 11, wherein the device is devoid of wire bonds, TAB leads and solder joints.

21. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and uncurved peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that provides the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, is farther from the bottom surface than the lower surface is from the bottom surface, provides at least a portion of the top surface and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

22. The device of claim 21, wherein the first housing portion contacts the lower surface and the outer side surfaces and is spaced from the upper surface.

23. The device of claim 21, wherein the second housing portion contacts the light sensitive cell and the conductive trace and is spaced from the lower surface.

24. The device of claim 21, wherein the first housing portion includes a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion is located within and recessed relative to the peripheral ledge.

25. The device of claim 21, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

26. The device of claim 21, wherein the insulative housing consists of the first and second housing portions.

27. The device of claim 21, wherein the light sensitive cell contacts a major surface of the second housing portion that faces towards and is parallel to the upper surface.

28. The device of claim 21, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

29. The device of claim 21, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

30. The device of claim 21, wherein the device is devoid of wire bonds, TAB leads and solder joints.

31. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive cell and is non-transparent, and the second housing portion is a single-piece or double-piece that provides a central portion of the top surface within the peripheral portion of the top surface, contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from the lower surface, is farther from the bottom surface than the lower surface is from the bottom surface, is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

32. The device of claim 31, wherein the second housing portion includes first and second opposing surfaces, the first surface faces towards the chip and contacts the light sensitive

cell and is spaced from the conductive trace, and the second surface faces away from the chip and provides the central portion of the top surface and is exposed.

33. The device of claim 31, wherein the peripheral portion of the top surface forms a rectangular peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

34. The device of claim 33, wherein the peripheral ledge includes four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

35. The device of claim 31, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

36. The device of claim 31, wherein the insulative housing consists of the first and second housing portions.

37. The device of claim 31, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed.

38. The device of claim 31, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

39. The device of claim 31, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

40. The device of claim 31, wherein the device is devoid of wire bonds, TAB leads and solder joints.

41. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing further includes a first insulative housing portion that covers the lower surface and is non-transparent and a second insulative housing portion that covers the light sensitive cell and is transparent; and

a conductive trace that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the conductive trace includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and the top surface.

42. The device of claim 41, wherein the first housing portion contacts the lower surface and four outer side surfaces of the chip.

43. The device of claim 41, wherein the second housing portion contacts the light sensitive cell and the conductive trace.

44. The device of claim 41, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

45. The device of claim 41, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

46. The device of claim 41, wherein the insulative housing consists of the first and second housing portions.

47. The device of claim 41, wherein the light sensitive cell contacts a major surface of the second housing portion that faces towards and is parallel to the upper surface.

48. The device of claim 41, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

49. The device of claim 41, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

50. The device of claim 41, wherein the device is devoid of wire bonds, TAB leads and solder joints.

51. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing further includes a first single-piece housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second single-piece housing portion that contacts the first housing portion and the conductive trace and is transparent, the first housing portion alone provides the bottom surface, and the first and second housing portions in combination provide the top surface; and

a conductive trace that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the conductive trace includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, wherein the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the top surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and one of the outer surfaces of

the recessed and non-recessed portions that face in the same direction as the top surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another.

52. The device of claim 51, wherein the second housing portion includes first and second opposing surfaces, the first surface contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

53. The device of claim 51, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

54. The device of claim 53, wherein the peripheral ledge includes four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

55. The device of claim 51, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

56. The device of claim 51, wherein the insulative housing consists of the first and second housing portions.

57. The device of claim 51, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

58. The device of claim 51, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

59. The device of claim 51, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

60. The device of claim 51, wherein the device is devoid of wire bonds, TAB leads and solder joints.

61. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

62. The device of claim 61, wherein the first housing portion contacts the lower surface and the side surfaces.

63. The device of claim 61, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

64. The device of claim 61, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the

recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

65. The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

66. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, is bent outside the insulative housing and is electrically connected to the pad inside the insulative housing.

67. The device of claim 66, wherein the first housing portion contacts the lower surface and the side surfaces.

68. The device of claim 66, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

69. The device of claim 66, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-

recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

70. The device of claim 66, wherein the device is devoid of wire bonds, TAB leads and solder joints.

71. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, does not contact an insulative material outside the first housing portion and is electrically connected to the pad inside the insulative housing.

72. The device of claim 71, wherein the first housing portion contacts the lower surface and the side surfaces.

73. The device of claim 71, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

74. The device of claim 71, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

75. The device of claim 71, wherein the device is devoid of wire bonds, TAB leads and solder joints.

76. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing.

77. The device of claim 76, wherein the first housing portion contacts the lower surface and the side surfaces.

78. The device of claim 76, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

79. The device of claim 76, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

80. The device of claim 76, wherein the device is devoid of wire bonds, TAB leads and solder joints.

81. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first and second housing portions, extends across one of the side surfaces and does not extend outside the insulative housing.

82. The device of claim 81, wherein the first housing portion contacts the lower surface and the side surfaces.

83. The device of claim 81, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

84. The device of claim 81, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

85. The device of claim 81, wherein the device is devoid of wire bonds, TAB leads and solder joints.

86. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first and second housing portions, overlaps the pad, extends across one of the side surfaces and does not extend outside the insulative housing.

87. The device of claim 86, wherein the first housing portion contacts the lower surface and the side surfaces.

88. The device of claim 86, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

89. The device of claim 86, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

90. The device of claim 86, wherein the device is devoid of wire bonds, TAB leads and solder joints.

91. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

92. The device of claim 91, wherein the first housing portion contacts the lower surface and the outer side surfaces.

93. The device of claim 91, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

94. The device of claim 91, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

95. The device of claim 91, wherein the device is devoid of wire bonds, TAB leads and solder joints.

96. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

97. The device of claim 96, wherein the first housing portion contacts the lower surface and the outer side surfaces.

98. The device of claim 96, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

99. The device of claim 96, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one

another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

100. The device of claim 96, wherein the device is devoid of wire bonds, TAB leads and solder joints.

101. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

102. The device of claim 101, wherein the first housing portion contacts the lower surface and the outer side surfaces.

103. The device of claim 101, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

104. The device of claim 101, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-

recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

105. The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

106. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

107. The device of claim 106, wherein the first housing portion contacts the lower surface and the outer side surfaces.

108. The device of claim 106, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

109. The device of claim 106, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

110. The device of claim 106, wherein the device is devoid of wire bonds, TAB leads and solder joints.

111. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, is located between the second housing portion and the chip inside the insulative housing, is spaced from the top surface and is electrically connected to the pad inside the insulative housing.

112. The device of claim 111, wherein the first housing portion contacts the lower surface and the outer side surfaces.

113. The device of claim 111, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

114. The device of claim 111, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

115. The device of claim 111, wherein the device is devoid of wire bonds, TAB leads and solder joints.

116. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that

contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing, includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

117. The device of claim 116, wherein the first housing portion contacts the lower surface and the outer side surfaces.

118. The device of claim 116, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

119. The device of claim 116, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

120. The device of claim 116, wherein the device is devoid of wire bonds, TAB leads and solder joints.

121. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

122. The device of claim 121, wherein the first housing portion contacts the lower surface and the outer side surfaces.

123. The device of claim 121, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

124. The device of claim 121, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

125. The device of claim 121, wherein the device is devoid of wire bonds, TAB leads and solder joints.

126. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

127. The device of claim 126, wherein the first housing portion contacts the lower surface and the outer side surfaces.

128. The device of claim 126, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

129. The device of claim 126, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-

recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

130. The device of claim 126, wherein the device is devoid of wire bonds, TAB leads and solder joints.

131. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

132. The device of claim 131, wherein the first housing portion contacts the lower surface and the outer side surfaces.

133. The device of claim 131, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

134. The device of claim 131, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

135. The device of claim 131, wherein the device is devoid of wire bonds, TAB leads and solder joints.

136. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

137. The device of claim 136, wherein the first housing portion contacts the lower surface and the outer side surfaces.

138. The device of claim 136, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

139. The device of claim 136, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

140. The device of claim 136, wherein the device is devoid of wire bonds, TAB leads and solder joints.

141. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the

peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

142. The device of claim 141, wherein the first housing portion contacts the lower surface and the outer side surfaces.

143. The device of claim 141, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

144. The device of claim 141, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

145. The device of claim 141, wherein the device is devoid of wire bonds, TAB leads and solder joints.

146. An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

147. The device of claim 146, wherein the first housing portion contacts the lower surface and the outer side surfaces.

148. The device of claim 146, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

149. The device of claim 146, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

150. The device of claim 146, wherein the device is devoid of wire bonds, TAB leads and solder joints.